Amendments to the Claims

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 4, 5, 9, 12, 17, 21, 22, 28, 29, and 30 have been amended. Claims 2-3, 13, and 23 have been canceled. Claims 31-41 have been added.

Listing of Claims:

1. (Currently Amended) An apparatus comprising:

a functional redundancy checking (FRC) processor including:

~~an execution core~~ first and second execution cores to operate in FRC mode;

a ~~scan chain~~ first and second scan chain corresponding to the first and second execution cores to transfer data to one or more nodes of the first and second execution ~~core~~ cores; and

a reset module including a pattern generator to store and ~~to~~ provide [[a]] an identical bit pattern to the first and second scan ~~chain~~ chains, responsive to a reset signal.

2. (Canceled)

3. (Canceled)

4. (Currently Amended) The apparatus of claim [[3]] 1, wherein the reset module drives the first and second scan chains in parallel.

5. (Currently Amended) The apparatus of claim 1, wherein the reset module further comprises:

a clock mux to provide a first or second clock signal to the scan chain, responsive to a reset signal~~; and~~.

~~a pattern generator to store the bit pattern and to provide the bit patter pattern to the scan chain, responsive to the reset signal.~~

6. (Original) The apparatus of claim 5, wherein the reset module further comprises a mode selector to assert a signal to the clock mux and the pattern generator, responsive to assertion of the reset signal.

7. (Original) The apparatus of claim 1, further comprising a reset tree to propagate voltage states to selected nodes of the execution core, responsive to the reset signal.

8. (Original) The apparatus of claim 1, further comprising a storage device to store a reset code module, the reset code module to step the execution core through a sequence of operations to establish states for additional nodes of the execution core.

9. (Currently Amended) A method for resetting a multicore FRC processor comprising:

detecting a reset event;

generating a bit pattern in a reset module of the multicore FRC processor;

applying [[a]] the bit pattern to a corresponding scan chain in each of the execution cores of the processor, the bit ~~patter~~ pattern to drive specified states to one or more processor nodes accessible through the scan ~~chain~~ chains.

10. (Original) The method of claim 9, wherein applying the bit pattern comprises:

applying a scan clock to a clock line of the scan chain; and

applying the bit pattern to a data line of the scan chain.

11. (Original) The method of claim 9, further comprising propagating the reset signal to selected nodes of the processor through a reset tree.

12. (Currently Amended) The ~~processor~~ method of claim 11, further comprising executing a reset code module to place additional nodes of the processor into specified states.

13. (Canceled)

14. (Original) The method of claim 11, wherein applying the bit pattern to a corresponding scan chain in each execution core comprises applying the bit pattern in parallel to the corresponding scan chains.

15. (Original) The method of claim 9, further comprising detecting an operating mode for the processor.

16. (Original) The method of claim 15, wherein detecting the operating mode comprises determining if the operating mode is a high performance mode or a high reliability mode, and applying a bit pattern to the scan chain comprises applying a bit pattern to the scan chain if the determined mode is the high reliability mode.

17. (Currently Amended) A system comprising:

a processor including:

first and second execution cores to be operated in an FRC mode, responsive to a mode bit, each of the execution cores including a scan chain to transfer data to a first set of nodes of the execution core;

an FRC checker to be activated in FRC mode to compare data from the first and second execution cores; and

a reset module to apply a bit pattern to the scan chains of the first and second execution cores, responsive to a reset event in the system.

18. (Original) The system of claim 17, wherein the reset module includes a pattern generator to drive the bit pattern on data lines of the scan chains of the first and second execution cores responsive to a scan clock.

19. (Original) The system of claim 18, further comprising a reset tree, the reset tree including electrical connections to a second set of nodes to drive the second set of nodes to specified states responsive to the reset event.

20. (Original) The system of claim 18, further comprising a storage device to store a reset code module, the reset code module to be executed by the first and second execution cores to drive a third set of nodes to specified states, responsive to the reset event.

21. (Currently Amended) The system of claim 20, wherein the first, second, and third sets of nodes are mutually exclusive.

22. (Currently Amended) An apparatus comprising:

a FRC processor including,

~~an execution core including~~ a first and second execution core to operate in FRC mode, each having a set of voltage nodes coupled through data and clock lines; and

a reset module, including a pattern generator, to drive a data signal and a clock signal to the ~~set~~ sets of voltage nodes, responsive to occurrence of a reset event, the data signal to place the voltage nodes of the ~~set~~ sets in specified logic states.

23. (Canceled)

24. (Currently Amended) The apparatus of claim ~~23~~ 22, wherein the data signal driven by the reset module is a bit pattern that places the set of voltage nodes of the first and second execution cores in the specified logic states.

25. (Original) The apparatus of claim 24, wherein the reset module drives the set of voltage nodes of the first and second execution cores in parallel.

26. (Currently Amended) The apparatus of claim 22, wherein the first and second execution ~~cores~~ cores ~~comprises first and second execution cores, each having a set of voltage nodes, the first and second execution cores~~ to be operated in an FRC mode, responsive to a mode bit being in a first state.

27. (Original) The apparatus of claim 26, wherein the reset module is disabled and the execution cores are operated in a non-FRC mode, responsive to the mode bit being in a second state.

28. (Currently Amended) The apparatus of claim 22, further comprising a reset tree to drive a second set of voltage nodes of the apparatus to second logic states, responsive to occurrence of ~~a~~ the reset event.

29. (Currently Amended) The apparatus of claim 28, further comprising a storage device to store a reset code module, the reset code module to be executed by the execution ~~core~~ cores to place a third set of voltage nodes in each of the execution cores in specified logic states, responsive to the reset event.

30. (Currently Amended) The apparatus of claim 29, wherein the reset module establishes specified logic states for the first ~~set~~ sets of voltage nodes before the reset code module is executed.

31. (New) A multicore processor comprising:

a first and second execution core to operate in a functional redundancy checking (FRC) mode;

a first and second scan chains corresponding to the first and second execution cores to transfer data to one or more nodes of the first and second execution cores;

a FRC boundary checker to compare nodes of the first and second execution cores; and

an internal reset module, including a pattern generator to store a bit pattern, to provide the bit pattern to the first and second scan chains to put the first and second execution cores into a deterministic state responsive to a reset signal generated upon detection of a mismatch by the FRC boundary checker.

32. (New) The apparatus of claim 31, wherein the reset module drives the first and second scan chains in parallel.

33. (New) The apparatus of claim 31, wherein the reset module further comprises:

a clock mux to provide a first or second clock signal to the scan chains responsive to a reset signal.

34. (New) The apparatus of claim 34, wherein the reset module further comprises a mode selector to assert a signal to the clock mux and the pattern generator, responsive to assertion of the reset signal.

35. (New) The apparatus of claim 31, further comprising a storage device to store a reset code module, the reset code module to step the execution cores through a sequence of operations to establish states for additional nodes of the execution cores.

36. (New) The apparatus of claim 31, further comprising a reset tree to propagate voltage states to selected nodes of the execution cores, responsive to the reset signal.

37. (New) A method for resetting a functional redundancy checking (FRC) processor comprising:

performing a deterministic hardware reset in the FRC processor, the performing including,

performing functional redundancy boundary checking;

generating a reset event upon a functional redundancy boundary checking mismatch;

generating a bit pattern responsive to the reset event; and

driving the bit pattern into scan chains.

38. (New) The method of claim 37 wherein the processor includes multiple execution cores to operate in FRC mode and wherein the driving the bit pattern comprises applying the bit pattern to a corresponding scan chain in each of the execution cores.

39. (New) The method of claim 38, wherein the applying the bit pattern to a corresponding scan chain in each execution core comprises applying the bit pattern in parallel to the corresponding scan chains.

40. (New) The method of claim 37, further comprising the preliminary operation of:

detecting the FRC processor is in a high reliability mode, wherein the processor can operated in the high reliability mode or a high performance mode.

41. (New) The method of claim 37, wherein the performing further comprises propagating deterministic states through a reset tree to other processor nodes.